In the claims:

1. A bi-directional high speed video data transmission system, comprising:

a transmitter operative to receive and transmit a first video data stream;

a data pair connected to the transmitter, operative to relay the first video data stream from the transmitter;

a receiver connected to the data pair and operative to receive the first video data stream relayed by the data pair;

a first and second summing resistor connected to the data pair, the first and second summing resistor operative to convert a current transmitted across the data pair to a DC return current;

a return transmitter connected to the first and second summing resistor and operative to receive the DC return current and a return video data stream, further operative to transmit the return video data stream;

a return data pair connected to the return transmitter, operative to relay the return serial video data stream from the transmitter; and

a return receiver connected to the return data pair and operative to receive the return video serial data stream, the return receiver further connected to the transmitter.

2. The bi-directional high speed video data transmission system of claim 1, wherein:

the data pair comprises a first and second data line;

the return data pair comprises a first and second return data line;

the transmitter transmits the first video data stream by switching a DC-balanced current between the first and second data line, thus creating a first and second AC current on the first and second data line;

the first and second summing resistor convert the current transmitted across the data pair to a DC return current by merging the first AC current with the second AC current; and

the return transmitter transmits the return video data stream by switching the DC return current between the first and second return data line, thus creating a first and second AC return current on the first and second return data line.

3. The bi-directional high speed video data transmission system of claim 2, further comprising a filter connected between the first and second summing resistor and the return transmitter.

4. The bi-directional high speed video data transmission system of claim 3, wherein the filter eliminates line noise present in the DC return current.

5. The bi-directional high speed video data transmission system of claim 3, wherein the filter is an LC filter.

6. The bi-directional high speed video data transmission system of claim 2, further comprising:

a first clock signal having a regularly repeating digital clock pulse;

the transmitter operative to regulate the switching of the DC-balanced current between the first and second data line according to the digital state of the clock pulse; and

the return transmitter operative to regulate the switching of the DC return current between the first and second return data line according to the digital state of the clock pulse.

7. The bi-directional high speed video data transmission system of claim 2, further comprising:

a first clock signal having a first period;

the transmitter further operative to regulate the switching of the DC-balanced current between the first and second data line according to the digital state of the first clock pulse;

a second clock signal having a second period of different duration than the first period;

the return transmitter further operative to regulate the switching of the DC return current between the first and second return data line according to the digital state of the clock pulse.

8. The bi-directional high speed video data transmission system of claim 6, wherein:

the transmitter regulates the switching of the DC-balanced current between the first and second data line by switching the DC-balanced current at a time corresponding to a first edge of the clock pulse; and

the return transmitter regulates the switching of the DC return current between the first and second data line by switching the DC return current at a time corresponding to a second edge of the clock pulse.

9. A video camera incorporating the bi-directional high speed video data transmission system of claim 2.

10. A computer video system incorporating the bi-directional high speed video data transmission system of claim 2.

11. The bi-directional high speed video data transmission system of claim 2, further comprising a first and second return summing resistor connected between the return data

pair and the transmitter, the first and second return summing resistor operative to merge the AC current transmitted across the first return data line with the AC current transmitted across the second data line into a DC current.

12. The bi-directional high speed video data transmission system of claim 11, wherein:

the transmitter, return receiver, and first and second return summing resistor comprise a first transceiver;

the return transmitter, receiver, and first and second summing resistor comprise a second transceiver; and

the circuitry of the first and second transceivers are identical.

13. A unidirectional high speed video data transmission system, comprising:

a first transition minimized differential signaling transmitter operative to transmit a first video data stream by alternating a DC current between a first and second data line;

a data pair comprised of the first and second data line and having a first and second end, the data pair connected to the first transition-minimized differential signaling transmitter at the first end, the data pair further connected to a first transition-minimized differential signaling receiver at the second end, the data pair operative to relay the first video data stream from the first transmitter to the first receiver;

the first transition-minimized differential signaling receiver operative to receive and output the first video data stream;

a first summing resistor connected to the first data line;

a second summing resistor connected to the second data line;

the first and second summing resistors comprising a first summing pair operative to merge the alternating current across the first and second data lines to form a DC return current;

a second transition minimized differential signaling transmitter operative to transmit a second video data stream by alternating a second DC current between a third and fourth data line;

a second data pair comprised of the third and fourth data line and having a first and second end, the second data pair connected to the second transition-minimized differential signaling transmitter at the first end, the second data pair further connected to a second transition-minimized differential signaling receiver at the second end, the second data pair operative to relay the second video data stream from the second transmitter to the second receiver;

the second transition-minimized differential signaling receiver operative to receive and output the second video data stream;

a third summing resistor connected to the third data line;

a fourth summing resistor connected to the fourth data line;

the third and fourth summing resistors comprising a second summing pair operative to merge the alternating current across the third and fourth data lines to form a DC final current;

wherein the DC return current and the second DC current are the same; and

wherein the third data line functions as a DC return channel.

14. The unidirectional high speed video data transmission system of claim 13, further comprising:

a clock signal having a regularly repeating digital clock pulse;

the first transition-minimized differential signaling transmitter operative to regulate the switching of the DC current between the first and second data line according to the digital state of the clock pulse; and

the second transition-minimized differential signaling transmitter operative to regulate the switching of the DC return current between the first and second return data line according to the digital state of the clock pulse.

15. The unidirectional high speed video data transmission system of claim 14, wherein:

the first transition-minimized differential signaling transmitter regulates the switching of the DC current between the first and second data line by switching the DC current at a time corresponding to a first edge of the clock pulse; and

the second transition-minimized differential signaling transmitter regulates the switching of the DC return current between the first and second data line by switching the DC return current at a time corresponding to a second edge of the clock pulse.

16. The unidirectional high speed video data transmission system of claim 15, further comprising a filter located between the first and second summing pairs, the filter operative to minimize line noise in the video data transmission system.

17. A method for enabling bi-directional high speed video data transmission, comprising the steps of:

receiving a parallel video data signal;

receiving a DC input current;

encoding the parallel video data signal as a serial video data signal;

transmitting the serial video data signal across a first and second data line by alternately transferring the DC input current between a first data line and a second data line to yield a first and second current, the first and second currents alternating between zero and a fixed value, the first and second currents one hundred eighty degrees out of phase with one another;

receiving the serial video data signal;

decoding the serial video data signal into the parallel video data signal;

summing the first and second currents into a DC return current;

receiving a return parallel video data signal;

encoding the return parallel video data signal as a return serial video data signal;

transmitting the return serial video data signal across a first and second return data line by alternating the DC return current across the first and second return data lines to yield a first and second return current, the first and second return currents alternating between zero and a fixed value, the first and second return currents one hundred eighty degrees out of phase with one another;

receiving the return serial video data signal; and

decoding the return serial video data signal into the return parallel video data signal.

18. The method of claim 17, further comprising the step of, in response to summing the first and second currents into a DC return current, filtering line noise from the DC return current.

19. The method of claim 17, further comprising the steps of:

summing the first and second return currents into a DC loop current; and

using the DC loop current as the DC input current.

20. The method of claim 17, further comprising the steps of:

receiving a clock signal having a rising edge and falling edge;

in response to receiving the rising edge of the clock signal, alternating the DC input current across the first and second data lines; and

in response to receiving the falling edge of the clock signal, alternating the DC return current across the first and second return data lines.